

JUL 12 2004

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INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

(Use as many sheets as necessary)

				Complete if Known	
		Application Number	10/681,108-Conf. #8110		
		Filing Date	October 9, 2003		
		First Named Inventor	Chandra Mouli		
		Art Unit	2011 <del>2829</del> 2891		
		Examiner Name	Not Yet Assigned		
Sheet	1	of	1	Attorney Docket Number	M4065.0762/P762

## U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.*	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code* (if known)			

## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.*	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>a</sup>
		Country Code* -Number-Kind Code* (if known)				

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## NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), data, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>a</sup>
LT	AA	P. BOULON et al., "Anomalous Short Channel Effects in Indium Implanted nMOSFETs," 1997 IEEE.	
LT	AB	Y. LEE et al., "Indium Doped nMOSFETs and Buried Channel pMOSFETs with n+ Polysilicon Gate," Jpn. J. Appl. Phys. Vol. 36 (1997), pp. 1341-1345.	
LT	AC	I. C. KIZILYALLI et al., "n+ Polysilicon Gate PMOSFET's with Indium Doped Buried-Channels," IEEE Electron Device Letters, Vol. 17 (1996), pp. 46-49.	
LT	AD	G. G. SHAHIDI, "Indium Channel Implants for Improved MOSFET Behavior at the 100-nm Channel Length Regime," IEEE Transactions on Electronic Devices, Vol. 36 (1989) p. 2605.	
LT	AE	H. TIAN et al., "A Comparative Study of Indium and Boron Implanted Silicon Bipolar Transistors," IEEE Transactions on Electron Devices, Vol. 48 (2001), pp.2520-2524	

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Luan Thai

3/14/05